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Sir:
Transmitted herewith for filing under 37 CFR 1.53(b) is the

[X] patent application of

Inventor(s)/Applicant Identifier: German Gutierrez

For: SEAL RING FOR INTEGRATED CIRCUITS

[X] This application claims priority from each of the following Application Nos./filing dates:
60/191,341/ Filed March 22, 2000
the disclosure(s) of which is (are) incorporated by reference.

Enclosed are:

[X] 5 page(s) of specification
[X] 4 page(s) of claims
[X] 1 page of Abstract
[X] 3 sheet(s) of [ ] formal [X] informal drawing(s).
[X] A [ ] signed [X] unsigned Declaration.

In view of the Unsigned Declaration as filed with this application and pursuant to 37 CFR §1.53(f), Applicant requests deferral of the filing fee until submission of the Missing Parts of Application.

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Attorney Docket No.: 19717-001510US
Client Reference No. NPC-15P (Parent)

PATENT APPLICATION

SEAL RING FOR INTEGRATED CIRCUITS

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SEAL RING FOR INTEGRATED CIRCUITS

CROSS-REFERENCES TO RELATED APPLICATIONS

This application claims priority from U.S. Provisional Patent Application Serial No. 60/191,341 filed March 22, 2000, the disclosure of which is incorporated herein by reference for all purposes.

BACKGROUND OF THE INVENTION

1. Field Of The Invention

The present invention relates generally to the manufacture of integrated circuits and more particularly, to a seal structure for a semiconductor die that improves substrate isolation.

2. Description Of The Prior Art

Most semiconductor integrated circuit manufacturers require a seal ring at the periphery of the semiconductor die. The seal ring circumscribes the periphery of the semiconductor die and is in contact with the die. The seal ring surrounds the bonding pads, which are typically disposed along the outer edges of the die. The seal ring creates a barrier to penetration of moisture, corrosive gasses, and chemicals.

A conventional seal ring is a multi-layer structure composed of alternating conducting and insulating layers. Through each of the insulating layers run multiple vias which provide electrical paths between adjacent metal layers. The lowest layer of metal in the seal structure makes electrical contact with the substrate, which can be either p-type or n-type. This structure ensures that no oxide path is presented to the edges of the semiconductor die after the semiconductor die has been diced (i.e., cut into individual dies from a wafer).

While this seal structure provides an effective barrier to undesirable environmental effects, it presents a problem that can be severe in certain circuit applications. Specifically, the seal ring creates a substrate short-circuit path all the way around the semiconductor die because multiple sections of the semiconductor die make electrical contact with the seal ring. In the case of mixed signal integrated circuits, which integrate both analog and digital circuits on the same substrate, circuit designers take careful measures to isolate the noisy portions of the substrate that include the digital circuitry from the section of the substrate that carries the noise sensitive analog circuitry.

This is usually accomplished by placing substrate barriers and substrate islands around different parts of the circuitry in order to isolate the more noisy circuit areas of the substrate from other areas that are more noise sensitive.

Isolating different circuitry areas on the substrate is effective in terms of directly isolating various portions of the circuitry from each other, but it does not address the short-circuit path between different portions of the circuitry provided by the seal ring. The seal ring provides a very low resistance metal path between different areas of the circuitry around the periphery of the substrate. Providing this path on which noise can travel from noisy areas of circuitry to noise sensitive areas defeats the attempts made to directly isolate the noisy digital areas of the substrate from the more noise sensitive analog areas.

SUMMARY OF THE INVENTION

The present invention is directed to a seal structure and method for forming a seal structure for a semiconductor die. An elongate region that is electrically isolated from the remainder of the substrate, such as a well region of a conductivity type opposite that of the substrate, extends around the major portion of the periphery of the substrate. A gap is left between the two ends of the elongate region along the minor portion of the periphery of the substrate not covered by the elongate region. A conductive seal ring is formed around the periphery of the substrate at the elongate region and spans the gap between the ends of the elongate region. The substrate of the semiconductor die is only brought into electrical contact with the seal ring at the gap between the ends of the elongate region.

Allowing the substrate to electrically contact the seal ring only at a minor portion of the seal ring ensures that the short circuit between the seal ring and the substrate is limited to a small portion of the semiconductor die. Thus, the only low resistance electrical path between the substrate and the seal ring is confined to the small portion of the seal ring in electrical contact with the gap in the elongate region. With only one low resistance electrical path between the seal ring and the substrate, the seal ring no longer behaves as a conductive ring interconnecting all areas of the semiconductor die. The direct contact between the seal ring and the substrate at the gap is sufficient, however, to prevent the seal structure from accumulating charge while being manufactured. The location of the minor portion of the seal ring that contacts the substrate can be adjusted and optimized according to the specific circuit requirements.

For example, in some applications it might be desirable to place the portion of the seal ring that contacts the substrate near the noisy area, or vice versa.

As mentioned above, the substrate and the well region of the preferred embodiment are formed having opposite conductivity types. The present invention allows for the substrate to have either a p-type or n-type conductivity, and the elongate region may be a well having either an n-type or p-type conductivity, respectively. Forming a well region with a conductivity opposite that of the substrate of the semiconductor die, and bringing the majority of the seal ring into physical contact only with the well region, reduces the ability of the semiconductor to communicate electrical signals, more specifically noise, through the seal ring to noise sensitive areas of the semiconductor die, without diminishing the protective benefits of the seal ring during manufacture of the die and during use of the semiconductor.

Other embodiments that isolate the seal ring from all or most of the substrate are also possible. For example, instead of the elongate well region, a high quality dielectric may be placed under the seal ring to electrically isolate it from the substrate. In another embodiment, the seal ring is electrically isolated from the substrate along the entire periphery of the die, and a separate low resistance path is provided between the seal ring and a power supply node to avoid a floating seal ring.

The novel features that are characteristic of the invention, as to organization and method of operation, together with further objects and advantages thereof, will be better understood from the following description when considered in connection with the accompanying drawings in which a preferred embodiment of the invention is illustrated by way of example. It is to be expressly understood, however, that the drawings are for the purpose of illustration and description only and are not intended as a definition of the limits of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic cross sectional view of a prior art seal ring and substrate;

Fig. 2 is an overhead view of the prior art seal structure of Fig. 1; and

Fig. 3 is an overhead view depicting the preferred embodiments of the seal structure of the present invention.

DESCRIPTION OF THE SPECIFIC EMBODIMENTS

A prior art semiconductor die 210 employing a seal ring structure 200 formed on a substrate 208 is illustrated by way of reference to Figure 1. Seal ring 200 is composed of alternating conductive metal layers 203 and insulating layers 204. Each insulating layer 204 contains one or more vias 206 extending through the insulating layer and providing a conductive path between various metal layers 203. The lowest conductive metal layer 203' of seal 200 contacts substrate 208 through vias 206' to provide a relatively low resistance conductive path between the seal ring and the substrate of semiconductor die 210. Substrate 208 is typically silicon, but may consist of other materials.

Figure 1 shows substrate 208 as having a p-type conductivity. Alternatively, substrate 208 could have an n-type conductivity. In either event, substrate 208 is rendered partially conducting. Dicing discharging paths 212 are created in substrate 208 at the point at which the lowest conductive metal layer 203' of seal ring 200 contacts the substrate. Dicing refers to the industry process of configuring a wafer into individual dies. Discharge paths 212 discharge charge in the substrate which has accumulated during manufacture of the semiconductor die.

As illustrated in Figure 2, semiconductor die 210 has mixed signal integrated circuits, and two distinct circuit areas are located on substrate 208. Digital circuit area 214 contains a variety of digital circuits. Digital circuit area 214 is L shaped and occupies the majority of the area enclosed by seal 200. Analog circuit area 216 is also located on substrate 208 and contains a variety of analog circuits. Analog circuit area 216 is square and occupies the area enclosed by seal ring 200 not occupied by digital circuit area 214.

The digital circuits located in digital circuit area 214 characteristically create a relatively large amount of noise, to which the digital circuits themselves are not susceptible. The analog circuits in analog circuit area 216, however, are noise sensitive, i.e., they are prone to errors in the presence of noise. Digital circuit area 214 and analog circuit area 216 are prevented from transmitting noise directly to one another by substrate barriers or substrate islands (not shown) between the respective areas.

The region of the substrate 208 between the digital circuit area 214 and the conductive ring seal 200 provides partially conductive paths between the digital circuit area and the ring seal represented by resistor symbols 218. While the noise generated by the digital circuits is typically isolated so that it cannot directly reach the noise sensitive

analog circuits in analog circuit area 216, such noise can reach conductive seal ring 200 through the conductive paths in the substrate represented by resistor symbols 218.

Analog circuit area 216 has a plurality of dicing discharging paths represented by resistors 220 between the analog circuit area and seal ring 200. These dicing discharging paths 220 allow the noise generated by the digital circuit area 214 and carried on conductive ring seal 200 to enter analog circuit area 24. This prior art implementation of the seal ring thus has the undesirable effect of transmitting noise from relatively high noise digital circuits to noise sensitive analog circuits in mixed signal integrated circuits.

Figure 3 schematically illustrates a preferred embodiment of the semiconductor die 310 and seal ring 300 of the present invention. An elongate region 302 is formed in substrate 308 that extends around the majority of the periphery of semiconductor die 310. A gap 304 remains between the two ends 322, 323 of elongate region 302. In a preferred embodiment of the present invention, elongate region 302 constitutes an elongate well region having a conductivity type opposite from that of the substrate. If substrate 308 is p-type, the well region 302 is n-type, and vice versa. Alternatively, elongate region 302 may comprise a high quality dielectric layer that provides electrical insulation.

Seal ring 300 extends around the periphery of semiconductor die 310 and encompasses the digital circuit area 314 and the analog circuit area 316. The seal ring 300 of the preferred embodiment has the same structure as prior art seal ring 200 shown in Figure 1. Seal ring 300 physically contacts the substrate along the entire length of elongate region 302. Seal ring 300 also physically contacts the substrate at the gap 304 between the ends 322, 323 of elongate region 302. Substrate 308 makes electrical contact with seal ring 302 solely at the gap 304 where the substrate physically contacts the seal ring without the intervening well region 302 of opposite conductivity type (or other insulator). A single partially conducting path illustrated by resistor 325 extends through substrate 308 to the section of seal ring 302 in electrical contact with the substrate at gap 304.

The electrical conductivity between the digital circuit area 314 and the analog circuit area 316 is highly restricted by barriers and islands in the substrate, as illustrated by small resistor symbols 326. Elongate region 302 restricts the electrical contact between seal ring 300 and the digital and analog circuit areas 314 and 316 except at the gap 304 in the elongate region. Nonetheless, seal ring 302 prevents substrate 308

from accumulating charge during the manufacturing and dicing of semiconductor die 310. Although seal ring 300 is electrically isolated by elongate region 302, seal ring 300 maintains its ability to protect the various circuit areas from the penetration of moisture, corrosive gasses, and chemicals that might be present in the environment.

In operation, the digital circuits in digital circuit area 314 will create noise, which does not inhibit the proper operation of the digital circuits themselves. Features in substrate 308 between the respective areas will effectively prevent the noise generated by the digital circuits from reaching the noise sensitive analog circuits in analog circuit area 316. Because electrical contact between substrate 308 and seal ring 300 is inhibited by elongate region 302 except at the gap 304 located far from digital circuit area 314, the seal ring 302 does not provide a short circuit to transmit such noise and little of the noise generated by the digital circuits will reach analog circuit area 316. Yet, the limited electrical contact between substrate 308 and seal ring 300 at gap 304 allows the seal ring to perform its discharge function.

While a preferred embodiment of the present invention has been illustrated in detail, it is apparent that modifications and adaptations of that embodiment will occur to those skilled in the art. For example, while elongate region 302 has been shown as a well region, the elongate region could be a high quality dielectric region or other insulative feature and a separate low resistive path provided between the seal ring and a power supply node to avoid a floating seal ring. Also, the gap between the ends of the elongate region can be near or far from the noisy circuit areas as needs require. However, it is to be expressly understood that such modifications and adaptations are within the spirit and scope of the present invention, as set forth in the following claims.

WHAT IS CLAIMED IS:

1. A die seal structure for a semiconductor die having a substrate comprising:

an elongate region electrically isolated from the remainder of the substrate extending around a major portion of the periphery of the substrate and having a gap between ends of the elongate region along a minor portion of the periphery; and

a conductive seal ring extending around the entire periphery of the die in contact with the die at said elongate region and said gap to provide a limited electrical connection between the ring and the substrate at said gap.

2. The structure of claim 1 wherein the substrate has a first conductivity type, and wherein the elongate region comprises an elongate well region of a second conductivity type different from the conductivity of the first conductivity type.

3. The structure of claim 2 wherein the first conductivity type is p-type and the second conductivity type is n-type.

4. The structure of claim 2 wherein the first conductivity type is n-type and the second conductivity type is p-type.

5. The structure of claim 1 wherein the elongate region comprises an elongate dielectric region between the seal ring and the substrate.

6. The structure of claim 1 wherein the seal ring only electrically contacts the substrate of the semiconductor die at the gap.

7. The structure of claim 1 wherein the substrate is formed of silicon.

8. The structure of claim 1 wherein the conductive seal ring comprises a multilayer structure of alternating conducting and insulating layers, and wherein vias are formed in the insulating layers.

9. A method of sealing a semiconductor die having a substrate of a first conductivity type, comprising:

forming an elongate well region of a second conductivity type opposite from the first conductivity type extending around a major portion of the periphery of the

substrate and having a gap between ends of the well region at a minor portion of the periphery; and

placing a conductive seal ring extending around the entire periphery of the die in contact with said well region and said gap to provide limited electrical contact between the ring and the substrate of said first conductivity type at said gap.

10. The method of claim 9 wherein the substrate of the semiconductor die has an n-type conductivity and wherein said forming an elongate well region of a second conductivity type step includes forming an elongate well region of a p-type conductivity.

11. The method of claim 9 wherein the substrate of the semiconductor die an n-type conductivity and wherein said forming an elongate well region of a second conductivity type step includes forming an elongate well region of a p-type conductivity.

12. The method of claim 9 wherein the substrate of the semiconductor die is formed of silicon.

13. The method of claim 9 wherein said placing step includes sequentially forming a multiplicity of alternating conductive and insulative layers overlying one another, and forming vias in the insulating layers.

14. A die seal structure for a semiconductor die having a substrate of a first conductivity type, comprising:

an elongate well region of a second conductivity type opposite from the first conductivity type extending around a major portion of the periphery of the substrate and having a gap between the ends of the elongate region along a minor portion of the periphery; and

a conductive seal ring extending around the entire periphery of the die in contact with the die at said elongate well region and said gap to provide a limited electrical connection between the ring and the substrate of said first conductivity type at said gap.

15. The structure of claim 14 wherein the first conductivity type is p-type and the second conductivity type is n-type.

16. The structure of claim 14 wherein the first conductivity type is n type and the second conductivity type is p type.

17. The structure of claim 14 wherein the conductive seal ring comprises a multilayer structure of alternating conducting and insulating layers, and wherein vias are formed in the insulating layers.

18. A semiconductor device comprising:

a. a die including a substrate;

b. a die seal structure on the substrate, the structure comprising:

an elongate region electrically isolated from the remainder of the substrate extending around a major portion of the periphery of the substrate and having a gap between ends of the elongate region along a minor portion of the periphery; and

a conductive seal ring extending around the entire periphery of the die in contact with the die at said elongate region and said gap to provide a limited electrical connection between the ring and the substrate at said gap.

19. The structure of claim 18 wherein the substrate has a first conductivity type, and wherein the elongate region comprises an elongate well region of a second conductivity type different from the conductivity of the first conductivity type.

20. The structure of claim 18 wherein the first conductivity type is p-type and the second conductivity type is n-type.

21. The structure of claim 18 wherein the first conductivity type is n-type and the second conductivity type is p-type.

22. The structure of claim 18 wherein the elongate region comprises an elongate dielectric region between the seal ring and the substrate.

23. The structure of claim 18 wherein the seal ring only electrically contacts the substrate of the semiconductor die at the gap.

24. The structure of claim 18 wherein the substrate is formed of silicon.

25. The structure of claim 18 wherein the conductive seal ring comprises a multilayer structure of alternating conducting and insulating layers, and wherein vias are formed in the insulating layers.

26. The structure of claim 18 wherein the elongate region is isolated by oxide.

27. The structure of claim 26 wherein the conductive seal ring is connected to the substrate by a metal stub.

SEAL RING FOR INTEGRATED CIRCUITS

ABSTRACT OF THE DISCLOSURE

The present invention is directed to a seal structure and a method for forming a seal structure for a semiconductor die. An elongate region which is electrically isolated from the remainder of the substrate, such as a well region of a conductivity type opposite that of the substrate, extends around the major portion of the periphery of the substrate. A gap is left between the two ends of the elongate region along the minor portion of the periphery of the substrate not covered by the elongate region. A conductive seal ring is formed around the periphery of the substrate at the elongate region and spans the gap between the ends of the elongate region. The substrate of the semiconductor die is only brought into electrical contact with the seal ring at the gap between the ends of the elongate region.

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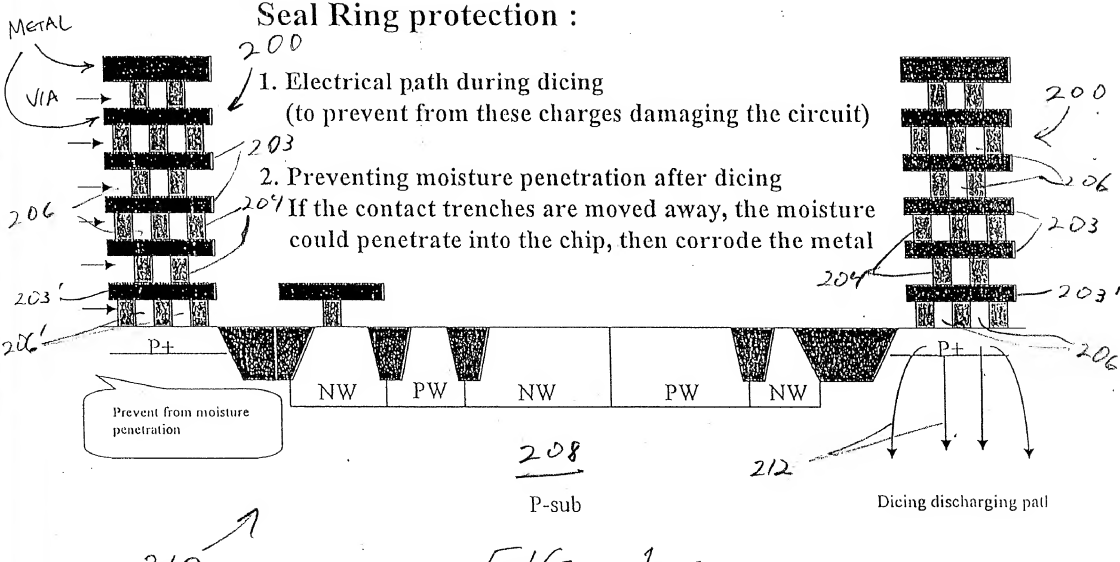
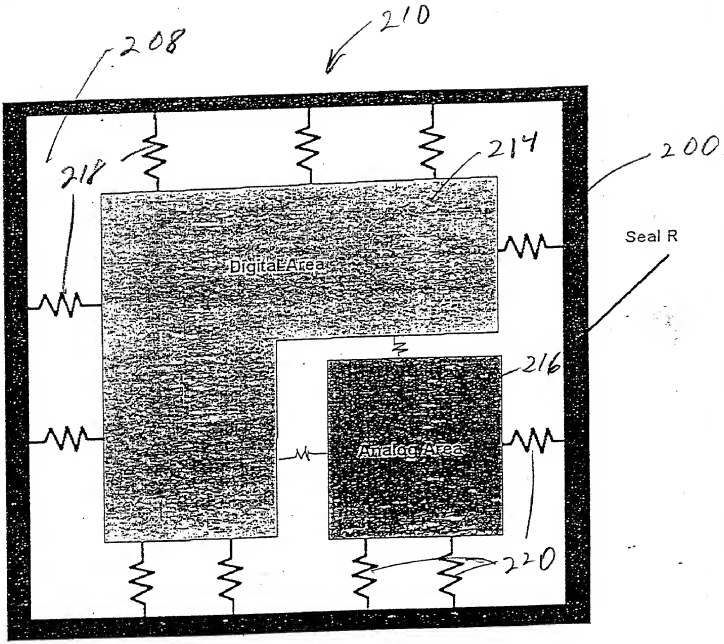
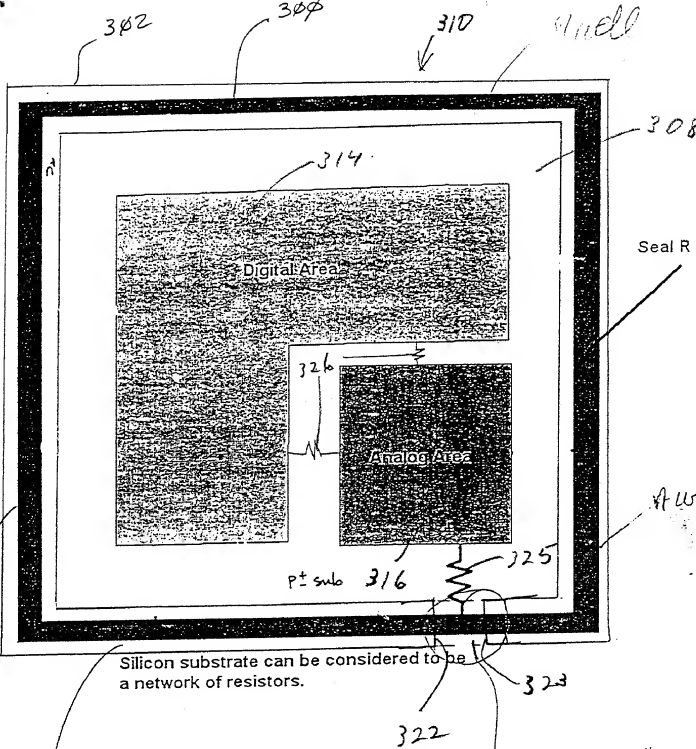


- FIG. 1 -



- FIG. 2 -


302
304
310
N well
308
314
Digital Area
Seal R
326
Analog Area
N well
325
P± sub
316
Silicon substrate can be considered to be a network of resistors.
323
322
304
regular seal ring substrate contact
N-well ring substrate

- FIG. 3 -

DECLARATION

As a below named inventor, I declare that:

My residence, post office address and citizenship are as stated below next to my name; I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural inventors are named below) of the subject matter which is claimed and for which a patent is sought on the invention entitled: **SEAL RING FOR INTEGRATED CIRCUITS** the specification of which __X__ is attached hereto or ____ was filed on _____ as Application No. _____ and was amended on _____ (if applicable).

I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56. I claim foreign priority benefits under Title 35, United States Code, Section 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

Country	Application No.	Date of Filing	Priority Claimed Under 35 USC 119

I hereby claim the benefit under Title 35, United States Code § 119(e) of any United States provisional application(s) listed below:

Application No.	Filing Date
60/191,341	March 22, 2000

I claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, Section 1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

Application No.	Date of Filing	Status

Full Name of Inventor 1:	Last Name: **GUTIERREZ**	First Name: **GERMAN**	Middle Name or Initial:	
Residence & Citizenship:	City: **Carlsbad**	State/Foreign Country: **California**	Country of Citizenship: **United States**	
Post Office Address:	Post Office Address: **1864 Palisades Drive**	City: **Carlsbad**	State/Country: **California**	Postal Code: **92008**

I further declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application or any patent issuing thereon.

Signature of Inventor 1
German Gutierrez
Date

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